Exercise 4: Transistor characterization and TLM

Location: MED 2 1519

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1. Summary

In this exercise you will perform the first set of characterizations on the devices prepared during the fabrication phase of this TP, resulting in MoS_2 devices with electrical contacts. While this and the next two exercises address different aspects and applications of nanoelectronic devices, the basic device for the applications considered here is a field-effect transistor with MoS_2 as the semiconductor channel.

After the previous exercise, the assistants have finished the lift-off step in the process and have also mounted the chip with the devices on a chip carrier (this step is referred to as packaging), and have performed wirebonding to connect the terminals on the chip carrier with the contact pads on the device. These steps are time-consuming and are outside of the scope of the TP, but the assistants would be happy to demonstrate them to you if you wish to know more.

The devices are now ready to be connected to instrumentation. We are going to make use here of high-end measurement instrumentation (a sourcemeter capable of measuring currents in the fA range), normally used in laboratories for measuring experimental nanoelectronic devices.

The main goal of this exercise is to carry out basic transistor electrical characterization and extract several parameters (contact resistance, mobility) that are usually employed for benchmarking transistors based on nanomaterials.

2. Background

2.1. Operation of a transistor based on a 2D material

Transistors based on MoS_2 behave as n-type field-effect transistors (FET), with the n-type doping predominantly coming from the presence of sulphur vacancies, with a concentration on the order of $\sim 10^{12} - 10^{13}$ cm^{-2}.

We can then represent them in a circuit schematic as shown on Figure 1a. G, D, and S correspond to gate, drain and source terminals, following the standard electrical-engineering convention in which source is the electrode emitting the majority charge carriers, in this case electrons (n-type doping). Following the same convention, the source is grounded and all the applied voltages are referenced to this terminal, so that V_{DS} is the drain source voltage (sometimes also referred to as the bias voltage), V_{GS} the gate voltage (sometimes written as V_G) and the current directions are as shown on Figure 1a. For simplicity, the symbol for the reference terminal (in this case the source) is often omitted, so that V_{DS} , V_{GS} , I_{DS} become V_D, V_G, I_D. In a good device I_{GS} (or simply I_{GS}) is expected to be small, ideally 0, and is referred to as the gate leakage current.

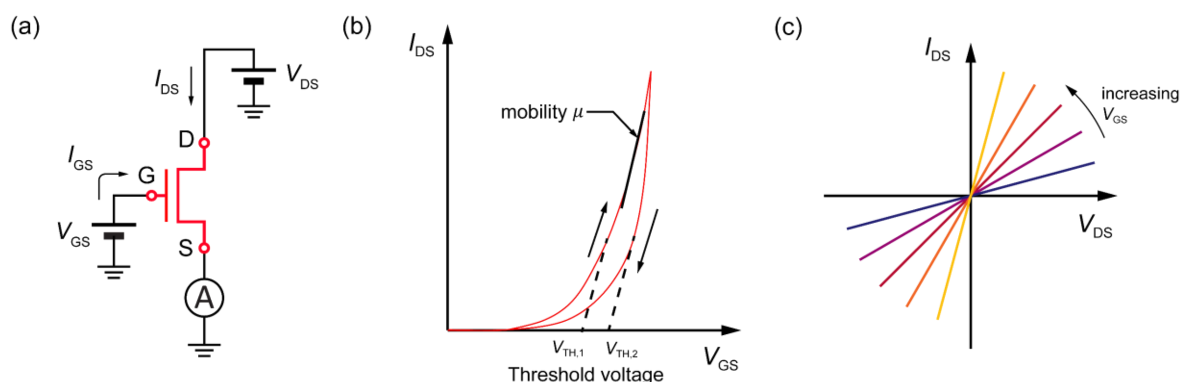


Figure 1. (a) Schematic of voltages and resulting currents in an n-type field-effect transistor. (b) Gating curve: I_{DS} as a function of V_{GS} for a certain value of V_{DS} (c) Biasing curve: I_{DS} as a function of V_{DS} for different values of V_{GS}.

Basic electrical characterisation of such n-type FETs then performed by measuring the drain current I_{DS} for different values of V_{DS} and V_{GS}. For acquiring gating curves such as the ones on Figure 1b, a bias voltage (for example V_{DS} = 100 mV) is applied to the drain terminal and the current is measured as the gate voltage is swept in a range of for example ±10 V. In the case of devices shown here it is recommended to keep the V_{DS} under 1V and $|V_{GS}|$<10V in order to prevent the dielectric breakdown of the gate dielectric insulator. The gating curve will in practice show hysteresis, since the channel can contains adsorbed water and oxygen molecules which can move and undergo electrochemical reactions. Because of this, the parameter extraction needs to be performed for the same direction of voltage sweeps (arrows on the graph in Figure 1b) or for both directions.

From the gating curve (Figure 1b), one can then extract the effective field-effect mobility μ_{FE} of the channel which is given by the formula:

$$\mu_{\mathrm{FE}} = \frac{dI_{\mathrm{DS}}}{dV_{\mathrm{GS}}} \frac{L}{W C_{\mathrm{G}} V_{\mathrm{DS}}} \tag{1}$$

where L is the channel length, W channel width, C_G the capacitance and V_{DS} the bias voltage. In principle, this mobility is then determined by making a linear fit in the region of the gating curve shown on Figure 1b. The formula is however only giving a lower limit since it is based on the assumption that the entire bias voltage drop V_{DS} occurs on the channel. This is equivalent to saying that the contact resistance $R_C = 0$ which is not the case, as you will see during this exercise. Threshold voltage can also be determined by extrapolating the same region of the gating curve to $I_{DS} = 0$.

The biasing curve (Figure 3c) is usually acquired for different values of V_{GS} for which the gating curve shows appreciable current. Its slope corresponds to the device resistance for the given V_{GS} which determines the doping level.

2.2. Transfer length method

One of the most straightforward methods for determining the contact resistance in nanoelectronic devices is the transfer length measurement (also referred to as the transmission line measurement). This measurement involves making a series of metal-semiconductor contacts with different contact separations and measuring the electrical resistance between them by applying a voltage and measuring the resulting current. Since this current is also dependent on the doping level of the semiconductor and the applied gate voltage, it is best practice to use measurements performed at the same gate voltage or same overdrive voltage ($V_{OV} = V_G - V_{TH}$) when performing the analysis.

Assuming that the total resistance of the device is the sum of the contact resistance and the resistance of the semiconductor, we can express the total resistance R_{tot}:

$$R_{tot} = \rho_{2D} \frac{L}{W} + 2R_C \tag{2}$$

where ρ_{2D} is the 2D electrical resistivity (in units of Ω), L device length, W device width and R_C contact resistance, corresponding to one of the contacts.

We also note that the electrical 2D electrical resistivity has the units of Ω which can be confusing at first. This is because the standard formula for electrical resistance of the material

$$R = \rho \frac{l}{S} = \rho \frac{l}{W \cdot t} \tag{3}$$

in 2D becomes

$$R_{2D} = \rho \frac{l}{W} \tag{4}$$

since in 2D we consider that materials do not have a thickness.

From Equation (2), we can see that the first term is proportional to length L while the second term is a constant. If we then measure and plot the total device resistance as a function of contact separation (or device length) as on Figure 2b. From the plot of R_{tot} as a function of L we can then extract $2R_C$ which corresponds to the intercept on the y axis.

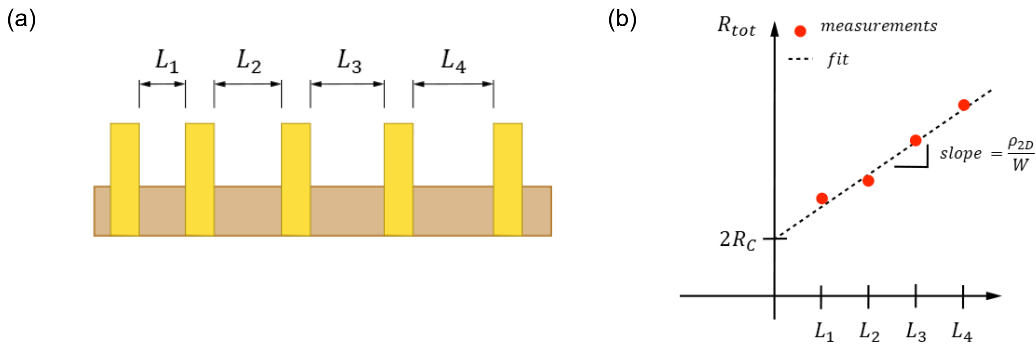


Figure 2. (a) Schematic drawing of a device for TLM measurements with different contact spacing. (b) Plot of R_{tot} as a function of L. The intercept on the y axis corresponds to $2R_C$.

2.4. Wire bonding and packaging

In order to connect the contact pads on the devices with the external electronics, the TA used the method called wire bonding and a wire bonder, Figure 3a. This is a common method for connecting integrated circuits to packages such as the one used in this exercise and shown on Figure 3b.

The wires used to make the connection have a diameter of 25 µm (for comparison, a typical diameter of a single hair is ≈ 80-100 µm) and are made of an alloy of aluminum and silicon (1%). During the wire bonding process, the user manipulates the tool wedge under a microscope. This wedge resembles a needle in a sewing machine with the thin wire in place of a thread. The hand motion of the operator is de-multiplied by a factor of 10, so that regular movements of the hand can be used to manipulate the tool under the microscope with sufficient precision. Once the sensor inside the tool detects mechanical contact with a contact pad, a short ultrasonic pulse is emitted which bonds the wire with the contact pad either on the chip or the package. The process is quite straightforward but requires some skill since a common beginner mistake is to apply too much pressure on the tip which can result in the failure of the insulating film under the contact pads and an electrical short circuit between the source/drain electrodes and the gate.

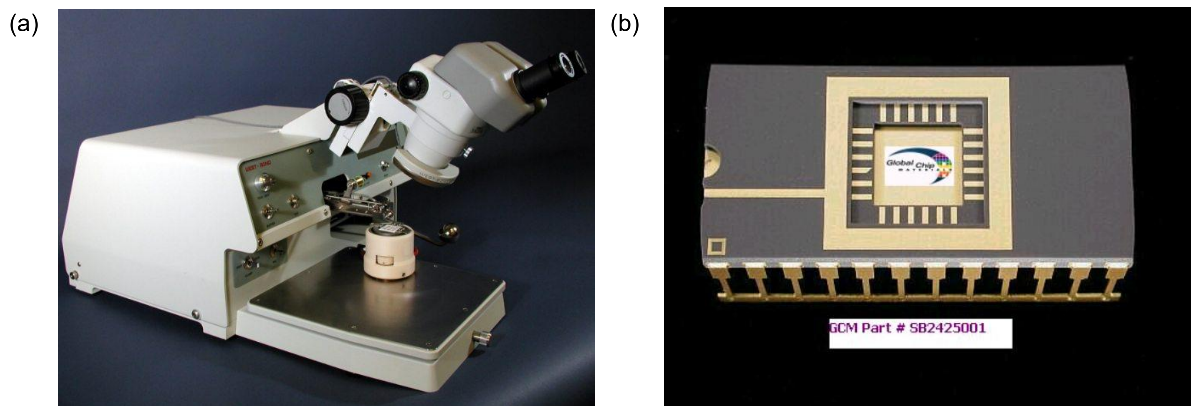


Figure 3. (a) Photo of a manual wire bonder from the company Westbond, utilized for preparing the chip used in this exercise. (b) Ceramic (mostly) chip package made by the company Kyocera, used in this exercise.

2.5. Electrostatic discharge

Electrostatic discharge (ESD) is an event in which static electricity from for example your clothes can be released. ESD can destroy delicate electronic devices such as the ones used in this and subsequent exercises. You have probably been zapped by such discharges when removing clothes for example. Such discharges involve potentials on the order of 100 V or even more (but the amount of charge is small so you do not get electrocuted). Smaller events, on the order of 10 V happen quite often but are normally not perceived. Those are still sufficient for destroying the devices by for example touching the chip with bare hands. Common methods or protection involve grounding equipment or yourself through a ~ 1MΩ resistor which decreases the currents associated with ESD but allows the efficient removal of charges.

In order to protect the devices from ESD, you will need to take several precautions. You will attach an antistatic wristband, which will effectively ground you. It then advised to handle the chips, wires, electrical cabling etc. with the hand on which you are wearing the bracelet. The work area is also going to have a grounded mat and the chip is also stored in an ESD-safe box, made of a conducting polymer.

2.6. Description of the equipment used

Keithley 2636B Sourcemeter

Figure 4. Front (left) and back (right) views of the Keithley 2636B 2-channel low-current sourcemeter.

The Model 2635B Sourcemeter from Keithley, a so-called source-measure unit (SMU instrument), combines high quality sources of current and voltage with precise measurements of the same, so that in a single channel you can for example apply a voltage and measure the current in the same time. The wide range of 1.5A DC, 10A pulse, 200V output (which we will not fully take advantage of here for safety reasons) and 0.1fA measurement resolution makes it ideal to test a wide range of lower current devices and materials. The Model 2635B has 6½-digit resolution, USB 2.0, ethernet and GPIB connectivity.

The instrument is connected to test fixtures using triaxial cables, in order to allow the high precision measurements of low currents.

Breakout box - test fixture

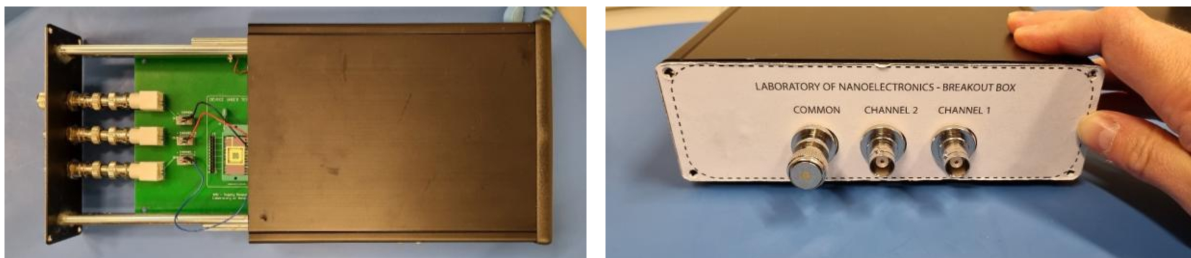


Figure 5. Top (left) and side (right) view of the breakout box that will be used in this exercise.

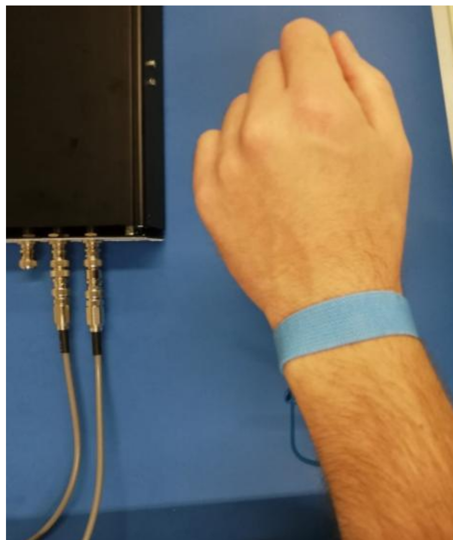
During the measurements, the chip with the mounted devices is kept in a breakout box whish allows interfacing the device with the measurement instrument. This box allows easily accessing the different contacts on the device and provides shielding from electromagnetic interference and light. On the front of the breakout box, we have three coaxial connectors which are connected to triaxial cables using adapters that leave the guard terminal floating. Channel 1 and 2 can be connected to the device terminal as well as the "Common" terminal which is connected to the reference terminal of the device and is connected to the shield of the triaxial cable using a grounding cap and closing the electrical circuit for measurements. The chip is placed into a ZIF (zero insertion force) socked on the board of the test fixture.

3. Description of experiments and tasks

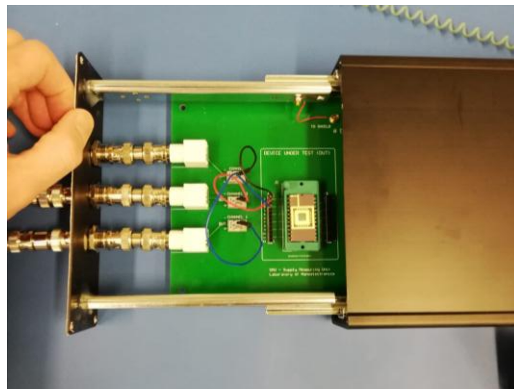
Following is the overview of the tasks and operations to be carried out in this exercise. The main goal is to perform electrical characterization of MoS_2-based transistors.

3.2. Setup – initial loading and handling of the chip with the device

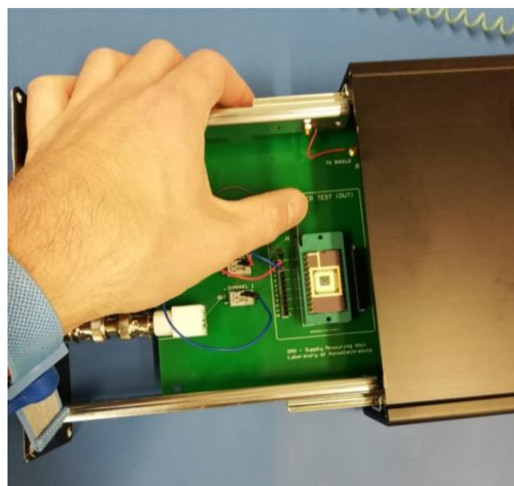
1. Ground yourself using the ESD Bracelet



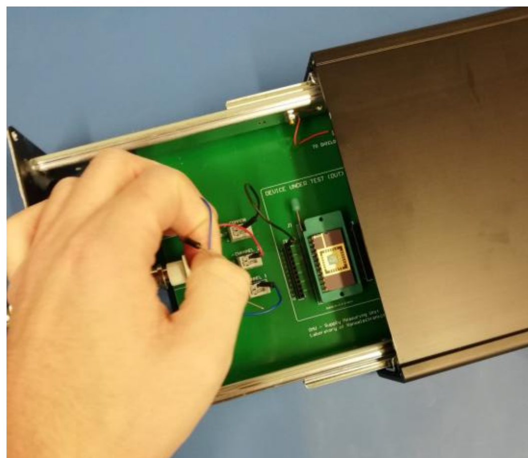
2. Open the breakout box and insert the device



3. Change the lever position on the ZIF socket to lock the device in place



4. Connect the jumpers to the pins corresponding to the chip legs that you would like to access.



3.3. Connecting an individual transistor device

The chip contains two devices for TLM measurements outlined on Figure 6 with contact pad numbers corresponding to the legs on the chip carrier and the pins in the breakout box.

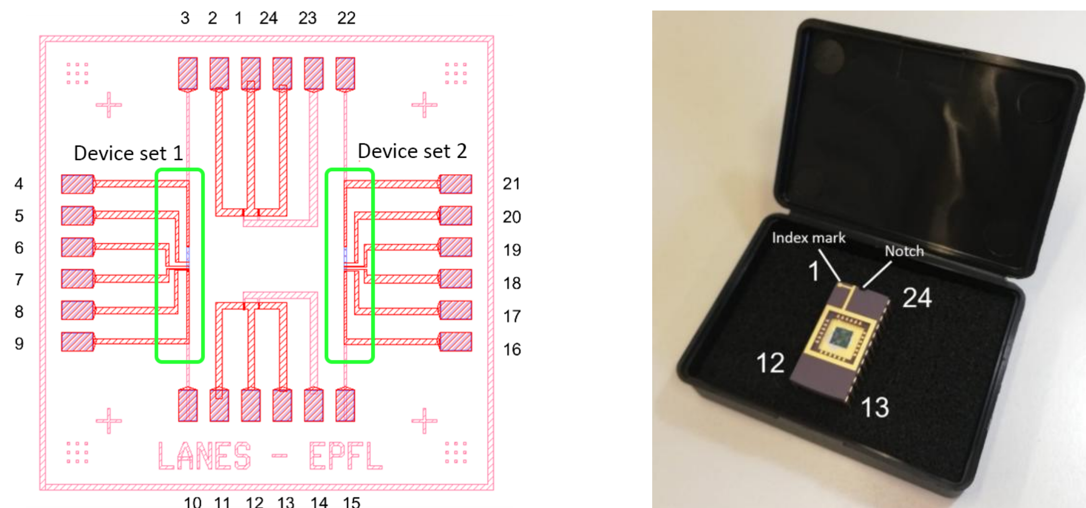
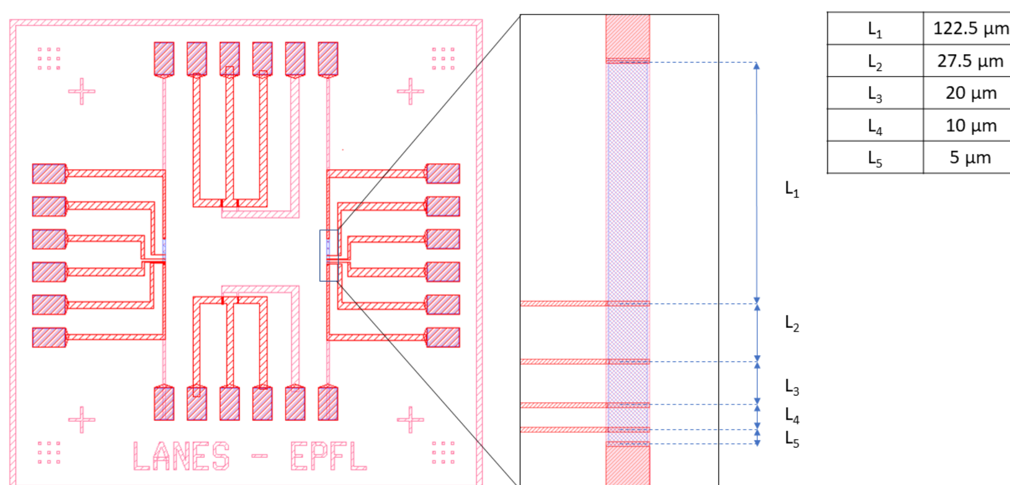


Figure 6. Left: schematic drawing of the device layout, with the corresponding pin numbering. There are two TLM devices. Device set 1 has the local back-gate connected to pins 3 and 10. Pins 4-9 correspond to electrical contacts. Neighboring pairs can be used as drain and source electrodes. Device set 2 has the local back-gate connected to pins 15 and 22. Pins 16-24 correspond to electrical contacts that can be used as drain and source electrodes. Right: photograph of a chip carrier package. The pins are numbered in a counter-clockwise direction, starting from pin 1 at the index mark (rectangle close to a corner of the chip).

By manually connecting the wires between the jumpers and the pins you can access the different devices on the chip.

The dimensions of the transistors in the TLM device set 2 are shown in Figure 7, device set 1 has the same dimensions.



L_1	122.5 µm
L_2	27.5 µm
L_3	20 µm
L_4	10 µm
L_5	5 µm

Figure 7. Channel lengths for the transistors in the TLM device set 1. Both TLM device sets (1 and 2) have the same dimensions. The channel width for all devices is 20 µm.

3.4. Familiarize yourself with the software interface

We will use a program in Labview for controlling the sourcemeter and measurement acquisition, with the interface shown in Figure 8.

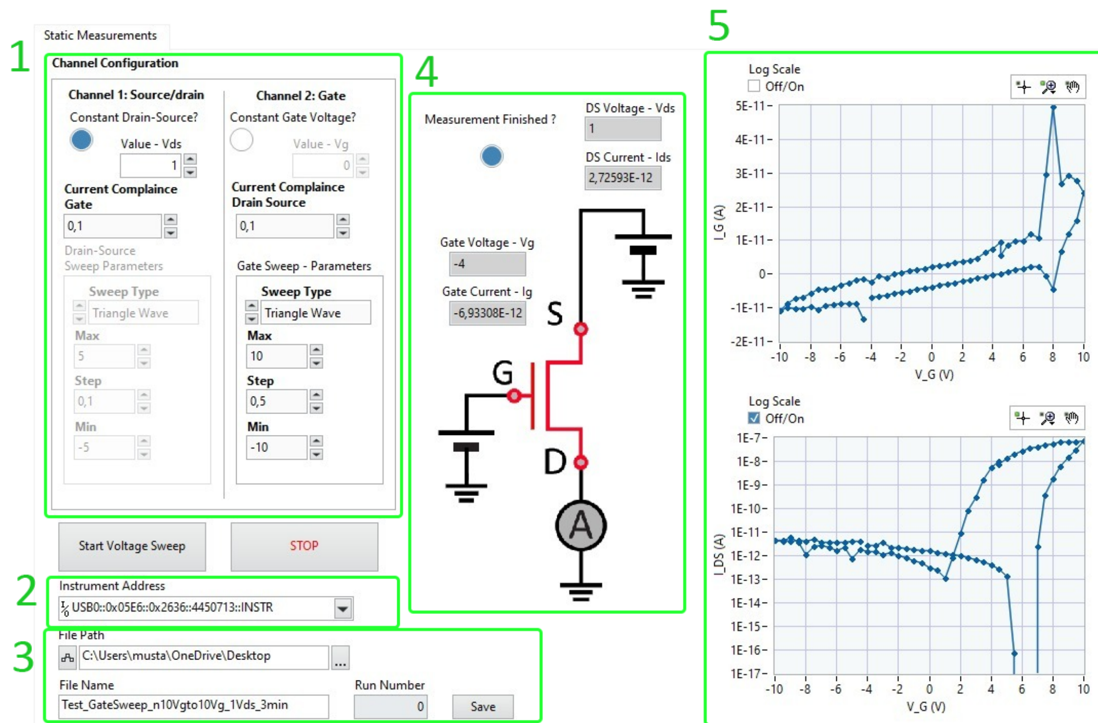


Figure 8. Interface for the data acquisition software used in this exercise.

Its main parts are:

1. Channel configuration
2. Instrument address
3. Path for saving the data
4. Schematic overview of the device and latest measurement values, together with an indicator showing if the current measurement has finished
5. Graphs with values from the current-voltage sweeps

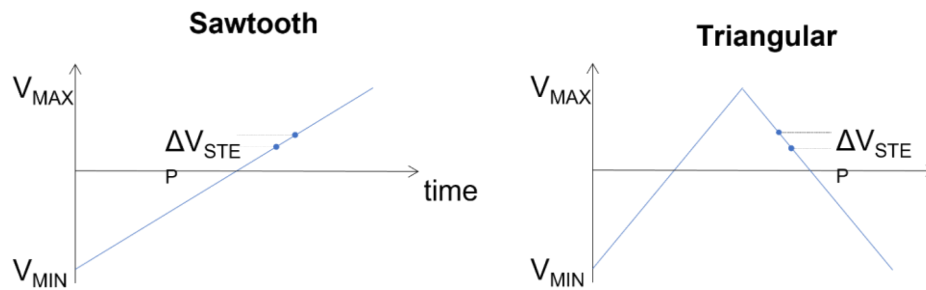
Configuring the instrument addres and file path

Scroll and select the first address and file path (folder in which want to save the file), enter a filename. To avoid overwritting a previously saved file, each time a file is saved, the run number is incremented and added to the end of the filename.

Configuring the voltage sweep

Here you can select the sweep type.

You can perform 2 types of sweeps, sawtooth or triangular:



When the configurations are ready, press Start Voltage Sweep. Stop will halt the software.

3.5. Perform device characterisation

1. **Transistor characterisation.** For the device with the shortest channel length, perform a full transistor characterisation:
   - measure I_{DS} vs. V_{GS} (gating curves) for V_{DS} =100 mV, 200 mV, 500 mV, 1V. Keep the V_{GS} in the ±10V range.
   - measure I_{DS} vs. V_{DS} (biasing curves) for V_{GS} = 0 V, 1, 2, 5 V. Keep the V_{DS} in the ±1V range.
   - from the measured curves, extract the estimated mobility, threshold voltages and hysteresis (defined as $V_{TH,2}-V_{TH,1}$, see Figure 1b).
2. **Transfer length method.** Perform TLM measurements on one of the device sets. For determining the resistance of an individual device, perform a gating curve measurement fist for a bias V_{DS} = 500 mV and calculate the contact resistances for V_{GS} = 5 V and V_{GS} = 8 V. Pay attention to the device hysteresis.

4. Questions for the report

In the report, please show and discuss the following:

1. A set of biasing and gating curves measured for the device with the shortest channel length. Show also the leakage current and compare with the off-state current of the transistor. Discuss possible origins for the observed leakage current.
2. Please show and discuss the extracted mobility and hysteresis. How would you reduce the hysteresis?
3. Extract the R_C and ρ_{2D} of the devices. How come these values depend on the gate voltage?